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AS8-static random access memory (SRAM): asymmetric SRAM architecture for soft error hardening enhancement

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Abstract: Soft errors in semiconductor memories occur due to charged particle strikes on sensitive nodes. Technology and voltage scaling increased dramatically the susceptibility of static random access memories (SRAMs) to soft errors. In this study, the authors present AS8-SRAM, a new asymmetric memory cell that enhances the soft error resilience of SRAMs by increasing the cells critical charge. They run Simulation Program with Integrated Circuit Emphasissimulations and system level experiments to validate the AS8-SRAM cell characteristics at circuit level and evaluate the energy and reliability effectiveness of an AS8-SRAM-based cache memory. The authors' results show that AS8-SRAM presents up to 58 times less failures in time compared to six-transistor SRAM. Moreover, based on embedded benchmarks experimentations, AS8-SRAM achieves up to 22% reduction in energy-delay product without any considerable loss in performance.

1 Introduction

Single event upsets (SEUs) result from a voltage transient event induced by alpha particles from packaging material or neutron particles from cosmic rays [1]. This event is created due to the collection of charge at a p–n junction after a track of electron–hole pairs is generated. A sufficient amount of accumulated charge in the struck node may invert the state of a logic device, such as a latch, static random access memory (SRAM) cell, or logic gate, thereby introducing an error into the hit circuit. In past technologies, this issue was considered in a limited range of applications in which the circuits are operating under aggressive environmental conditions like aerospace applications. Nevertheless, shrinking the transistor size and reducing the supply voltage in new technologies result in a remarkable decrease of the capacitance per transistor leading to a higher vulnerability within circuits nodes. Hence, SEUs become a challenging limitation of reliability in complementary metal–oxide–semiconductor (CMOS) circuits, especially for memories. Moreover, the Semiconductor Industry Association (SIA) roadmaps indicate that embedded memories are exceeding 90% of the chip area in the next few years [2]. Consequently, the overall systems reliability is considerably affected by the memory immunity to errors. Despite of the numerous published works, SRAM reliability enhancement is still an open problematic especially for new technologies.

The present work suggests a circuit-level technique to enhance the soft error resilience of SRAMs. We present AS8-SRAM, a new memory cell that enhances SRAM soft error immunity by increasing the cell critical charge. Simulation Program with Integrated Circuit Emphasis (SPICE) simulations show that AS8-SRAM almost doubles the six-transistor SRAM (6T SRAM) cell critical charge with acceptable access power overhead and negligible performance cost.

The remaining of the paper is organised as follows: Section 2 provides a background on the SRAM architecture and the soft error mechanism followed by an overview of related works dealing with soft error mitigation in SRAMs. The suggested architecture (AS8-SRAM) is detailed in Section 3. Next, in Section 4 we explain the experimental methodology used in this work and show the results. Finally, we conclude in Section 5.

2 Background and related work

6T-SRAM cells are memory cells built using a storage element and two access transistors. Fig. 1 shows a standard 6-T SRAM: the stored data is determined by the state of nodes S1 and S2. The storage nodes are formed by a pair of cross-coupled inverters and are accessed through two NMOS transistors (see Fig. 1). Consequently, if a particle-induced current appears in one of the cell's sensitive nodes (S1 or S2), it may propagate through the struck inverter and cause a transient noise on the second sensitive node. This will cause the second node to propagate the corrupted value, thereby flipping both nodes and by consequence, flipping the state of the bit stored in the SRAM cell. The minimum charge required to flip the cell is called the critical charge (Q_c) [3]. Hence, a soft error occurs when the charge resulting from the electron–hole pairs induced by an ionising particle, and collected at a junction, is greater than the hit node's critical charge. Numerous works have focused on soft error mitigation to limit SER in SRAMs.

Architecture level error resilience techniques like ECCs (error correcting codes) have been proposed and widely used [4]. The simplest form is the parity check method whose major weakness is its incapability to correct the detected errors [5]. Another form of ECC used in memories is the SECDED (single error correction, double error detection) [6]. The main problem of the SECDED is its area overhead and the supplementary latency leading to performance loss. A multi-copy cache (MC^2) fault tolerant memory has been proposed in [7]. The idea behind MC^2 is to exploit the cache area with multi-redundant lines in order to detect the possible faults and correct them by a majority vote. A fault tolerant architecture presented in [8] combines both parity and single redundancy to enhance memories reliability. In [9], two-dimensional matrix codes have been proposed to efficiently correct soft errors per word with a low delay. A combination of ECCs and a circuit level hardening technique is presented in [10]. The weakness of these techniques is their area, power and delay overheads due to the additional memory cells and supporting circuits required for error detection and correction.

Circuit level techniques have been proposed to overcome architecture level overheads. These techniques enhance soft error resilience in SRAM cells either by slowing down the response of

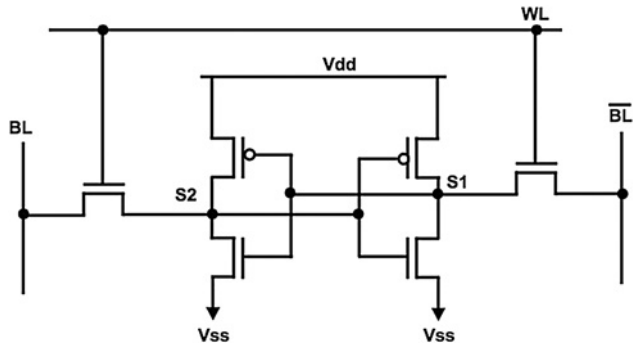


Fig. 1 *Standard 6T-SRAM cell circuit*

the circuit to transient events, or by increasing its Q_c. Upsizing the memory cells transistors increases the effective capacitance of the device and thus Q_c is also increased. This Q_c increment can make the cell less likely to be affected by the particle strike [11]. However, as it is shown in [12], the gain in cell robustness depends on the exact transistors that are upsized. Other methods such as [13] suggest to harden the cell using a pass transistor that is controlled by a refreshing signal. The authors of [14] add a redundant cross-coupled inverter to the 6T-SRAM to increase the cell critical charge. In [15], the authors proposed a quad-node 10-T memory cell which uses negative feedback to prevent memory bit flip. In [16], an 11-T single ended memory cell has been proposed to enhance soft error tolerance using refreshing mechanisms. Based on hysteresis effect of Schmitt trigger, Lin *et al.* [17] propose a hardened 13-T memory cell. However, this technique slows down the memory due to Schmitt trigger's hysteresis temporal characteristics. A modified hardened memory cell (RHM-12T) is proposed in [18] using 12 transistors. The following section details the proposed AS8-SRAM cell.

3 AS8-SRAM: asymmetric 8-T SRAM architecture

The more charge the strike-induced pulse injects into the SRAM cell, the more likely the stored data gets corrupted. In order to harden the SRAM cell against single event upsets (SEUs), the aim of AS8-SRAM is to create an internal resistance to the current pulse induced by the injected charge movements. In fact, the pulse induced in the output of the struck inverter is forwarded to the input of the second inverter. During this metastable state, the output of the second inverter strengthens the corrupted data until settling at a new stable erroneous state. If the critical charge of the SRAM cell is higher than the injected charge due to a charged particle hit, the induced glitch will disappear after the strike and the cell will restore its original state. Our approach is to present a radiation hardened architecture by attenuating the corrupting effect due to a particle strike by strengthening the original feedback cell mechanism.

AS8-SRAM architecture is designed to enhance the SRAM cell resilience at circuit level with the lowest possible overhead. As shown in Fig. 2, AS8-SRAM is different from 8T-SRAM [19] and is designed by adding a CMOS inverter in parallel with the storage element of the SRAM cell. The additional inverter's role is to resist to any metastable state caused by a particle strike induced pulse. In fact, the additional inverter increases the sensitive nodes capacitance and facilitates the initial data recovery by pulling the signal back to the initial correct state. Consequently, the impact of particle strikes on the AS8-SRAM is subdued and limited by the additional inverter effect. As a matter of fact, the minimum amount of collected charge needed to flip the stored data is increased by AS8-SRAM which enhances the immunity of the SRAM cell against soft errors. AS8-SRAM reliability enhancement level depends on the direction of the additional inverter vis-a-vis the struck node. Hence, we denote *direction 1* the case where the particle strike occurs in the node S1 that is driven by the additional inverter. *Direction 2* corresponds to a particle strike in the node S2. Despite the asymmetric aspect of the proposed cell, the reliability of the SRAM is enhanced in both directions.

As detailed in the following section, given that the signal states of the sensitive nodes are strengthened by AS8-SRAM, the read operation becomes faster. However, increasing the nodes capacitance results in a write time penalty that does not exceed 1/500 of the period for 1 GHz frequency. Moreover, to minimise the power consumption overhead due to the extra circuitry, the additional inverter's transistors are set to the minimum possible dimensions. In fact, both the N and P transistors have a width equal to the length: $L = W = 65$ nm. Notice that upsizing the additional inverter increases the Q_c and by consequence enhances the SRAM reliability. However, it results in performance loss, access time and power overhead increase. Hence, a tradeoff between the additional overheads and reliability has to be considered.

4 Experimental methodology

The Q_c of a memory cell is the minimum charge collected due to a particle strike which results in a bit flip. Therefore, the vulnerability of SRAM cells to soft errors is typically estimated based on its critical charge, Q_c [20]. The SER by cell decreases exponentially with the Q_c increase as shown in (1) below [21]

$$\mathrm{SER} = K \times \phi \times A \times \exp\left(-\frac{Q_c}{Q_s}\right) \tag{1}$$

where K is a proportionality constant, ϕ is the neutron flux with energy greater than 1 MeV, A is the sensitive area of the circuit and Q_s is the charge collection efficiency of the device, in fC. We model the soft error in SRAM cells by a current pulse injected into a sensitive cell node. Hence, we monitor the cell behaviour under particle strike by the observation of its SPICE simulation results. To highlight the reliability enhancement performed by AS8-SRAM architecture, we use the critical charge as an indicator of the memory cell resistance to particle strikes. We determine AS8-SRAM's critical charge at nominal voltage which corresponds to 1.1 V for 65 nm PTM [22] and track its under voltage scaling. We compare these results with the following cells:

- A standard 6T-SRAM cell.
- A 6T-SRAM cell with upsized transistor dimensions.

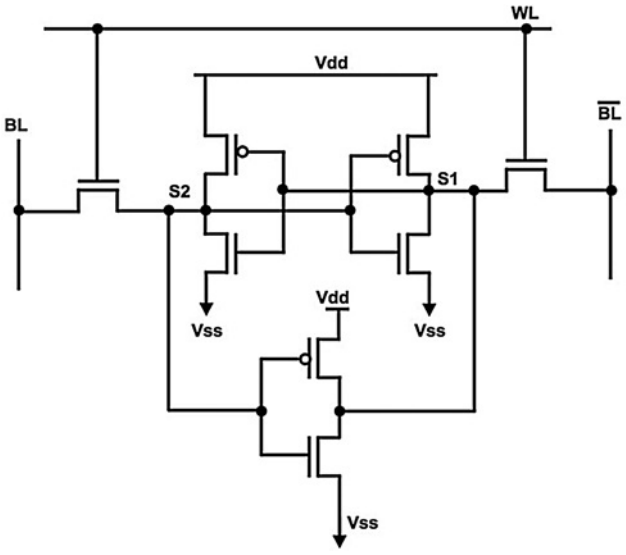


Fig. 2 *AS8-SRAM architecture*

Table 1 Sizes of the transistors used in the different tested memory cells

	NMOS width, nm	PMOS width, nm	Length, nm
Standard 6T-SRAM	260	177	65
upsized SRAM	291	209	65
AS8-SRAM[a]	65	65	65
3-eq-SRAM	195	139.5	65
4-eq-SRAM [14]	146.25	104.75	65

[a]Dimensions shown for AS8-SRAM correspond to the additional inverter. The transistor dimensions of the original cross coupled inverters are the same as 6T-SRAM

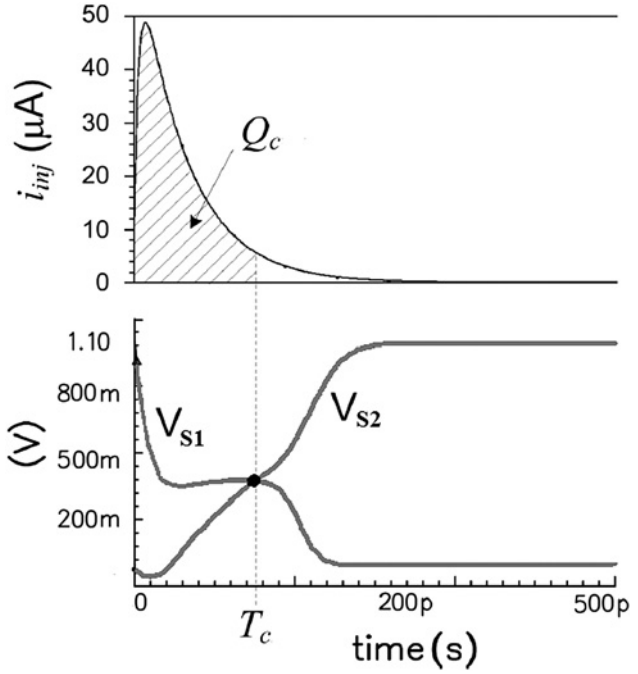


Fig. 3 *Graphical definition of critical charge. V_{S1} and V_{S2} are node S1 and S2 voltages, referencing Fig. 2*

- A 6T-SRAM cell with only 1 upsized inverter dimensions (referred to as 'upsized 1inv').
- 3-eq-SRAM: a hardened SRAM cell composed of three inverters with equivalent transistor dimensions.
- A soft error hardened SRAM cell proposed in [14] that we refer to as 4-eq-SRAM.

To insure a fair comparison, the three latter architectures are sized so that the overall cell area is equal to AS8-SRAM.

Table 1 details the sizes of the different transistors used in the architectures mentioned above. As the charge required for 1–0 transition is lower than the 0–1 transition, we considered the ?1? storage node for current injection.

In our experiments, we determine Q_c by injecting current pulses into the sensitive nodes of the memory cell. These pulses simulate the current induced by the particle strike. To calculate Q_c, we determine the minimum magnitude and duration of an injected current pulse that is sufficient to flip the data in the memory cell. Hence, Q_c is determined by integrating the current pulse corresponding to the smallest charge injected that flips the memory cell. Fig. 3 graphically illustrates the quantification of the cell Q_c. The critical time (T_c) is the time between the beginning of the current pulse and the intersection between the two cell nodes voltages. As shown in [15], we assume that once the memory cell reaches this state '$t = T_c$', the feedback between the cell nodes becomes strong enough to result in an erroneous stable state by flipping the initially stored data. Therefore, the injected charge until T_c is sufficient to flip the state of the cell and the critical charge is equal to the charge injected by the current pulse up to $t = T_c$

$$Q_c = \int_0^{T_c} i_{inj}(t)\,dt \tag{2}$$

where $i_{inj}(t)$ is the current pulse injected into the sensitive node to simulate the SEU.

System level simulations are also performed to show the impact of AS8-SRAM-based cache memory on energy consumption and reliability within a microprocessor architecture. We compare AS8-SRAM memory results with SECDED results from [7] for 65 nm technology.

The following section details and discusses the experimental results in terms of reliability and power/performance overhead.

5 Results

5.1 Reliability under nominal V_{dd}

To quantify the impact of the proposed architecture on the SRAM cell soft error resilience, we calculate the Q_c based on the simulation results and compare the AS8-SRAM Q_c with the different memory cell architectures mentioned in the previous section. Fig. 4 represents the Q_c corresponding to the different SRAM architectures fed by the nominal voltage for the 65 nm technology.

The results in Fig. 4 show that AS8-SRAM has the highest Q_c for both *direction 1* and *direction 2* of the additional inverter. In fact, in this case AS8-SRAM increases the critical charge of the standard 6T-SRAM cell by more than 95% in *direction 1* and 83% in *direction 2*. In terms of SER, (1) implies that the critical charge

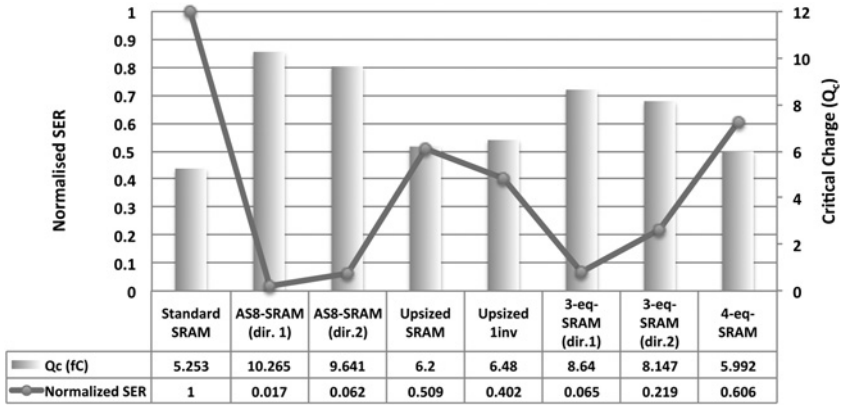
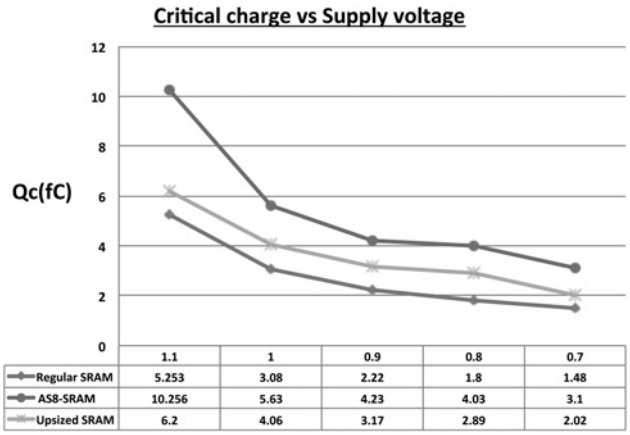


Fig. 4 *Critical charge and corresponding SER by cell for the different tested circuits under nominal V_{dd}*



	1.1	1	0.9	0.8	0.7
Regular SRAM	5.253	3.08	2.22	1.8	1.48
AS8-SRAM	10.256	5.63	4.23	4.03	3.1
Upsized SRAM	6.2	4.06	3.17	2.89	2.02

Fig. 5 *Critical charge against supply voltage scaling*

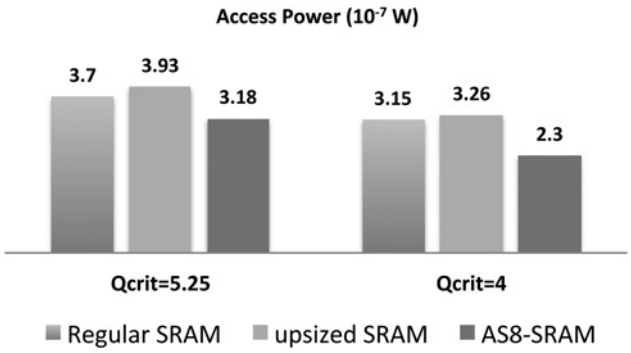


Fig. 7 *Access power by cell for different Q_c values*

augmentation corresponds to 58 times less failure in time compared to 6T-SRAM in *direction 1* and more than 16 times less in *direction 2*. We note that SER is calculated based on (1). As we calculate the normalised SER, the proportionality constant K disappears from the equation. The remaining parameters used to apply the SER model in our case are directly getting from [23]. The area ratios are calculated through the different designs cell areas.

5.2 Reliability under voltage scaling

Dynamic voltage scaling techniques are commonly used to reduce the power dissipation in memory architectures [24]. Nevertheless, in addition to the time penalty, reducing the supply voltage results in a higher cell sensitivity and by consequence increases the memories SER.

We performed a SPICE analysis to calculate Q_c of the different architectures operating under scaled supply voltages. Fig. 5 shows the critical charge of the 6T-SRAM, AS8-SRAM and the upsized SRAM in terms of the supply voltage. The results show that when $V_{dd} = 1$ V (scaled down by 9%), AS8-SRAM critical charge is almost equal to the standard SRAM's Q_c when operating under its nominal voltage. Besides, the results presented in Fig. 7 show that for the same reliability level AS8-SRAM is much more power efficient than the regular SRAM or the upsized SRAM. In fact, AS8-SRAM consumes 30% less power than the upsized SRAM and 27% less than the regular SRAM for $Q_c = 4$ fC. On the other hand, Figs. 6*a* and *b* show the performance comparison between AS8-SRAM, 6T-SRAM and the upsized SRAM for fixed Q_c values of 4 and 5.25 fC, respectively. The results show that AS8-SRAM has an average read time overhead of 6.35 and 4.075 ps, respectively, for $Q_c = 4$ fC and $Q_c = 5.25$ fC compared with the regular SRAM. For a frequency of 1 GHz, this overhead represents less than 0.7% of the period time.

To study the reliability of an AS8-SRAM-based memory, we compare the probability of failure (POF) of a 16 kB 4-way associative cache memory implemented with different technologies: conventional cache (CC) based on 6T-SRAM cells, a cache protected by SECDED [7] and an AS8-SRAM-based memory.
Let be:

- N: the number of SRAM cells in a cache memory.
- $p(V)$: POF of each 6T-SRAM cell at voltage V.
- $p_{AS8}(V)$: mean POF (between *direction 1* and *direction 2* of each AS8-SRAM cell at voltage V.

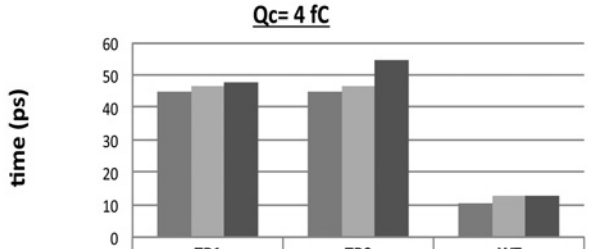
Hence, the POF of a conventional cache is expressed by the following equation

$$P_{cc} = 1 - (1 - p(V))^N \tag{3}$$

The POF of an AS8-SRAM-based memory $P_{AS8\text{-}mem}(V)$ can be expressed by the following equation

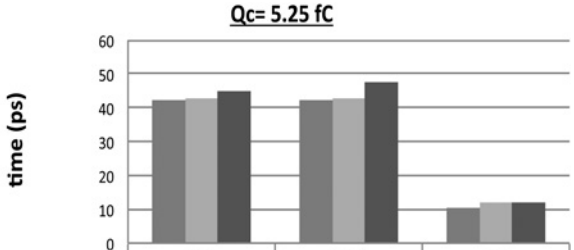
$$P_{AS8\text{-}mem}(V) = 1 - (1 - P_{AS8}(V))^N \tag{4}$$

Fig. 8 shows the POF comparison between the different technologies implementing a 16 kB 4-way associative cache memory. To perform a fair comparison, the cache memories results correspond to equal area for the three technologies. SECDED results are based on SPICE simulation with PTM [22] models taken from [7] for 65 nm. Fig. 8 shows that the implementation of a cache memory using AS8-SRAM cells carries out better reliability enhancement than SECDED for equal area. Moreover, unlike SECDED that needs additional circuitry to detect and correct errors, AS8-SRAM-based memory performs significant error probability reduction without changing the memory architecture.



	TR1	TR0	WT
Regular SRAM	45	44.8	10.6
upsized SRAM	46.5	46.4	12.7
AS8-SRAM	47.9	54.6	13

a



	TR1	TR0	WT
Regular SRAM	42.3	42.25	10.23
upsized SRAM	43	43	12.2
AS8-SRAM	45	47.7	11.8

b

Fig. 6 *Access time overhead for $Q_c = 4$ fC: TR1= time to read '1', TR0= time to read '0', WT= write time*

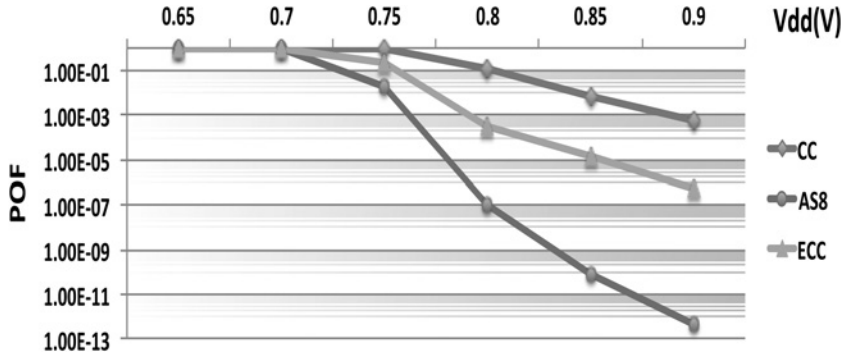


Fig. 8 *POF against V_{dd} for a 16 kB cache using: SECDED cache, CC and AS8-SRAM-based cache under iso-area constraint*

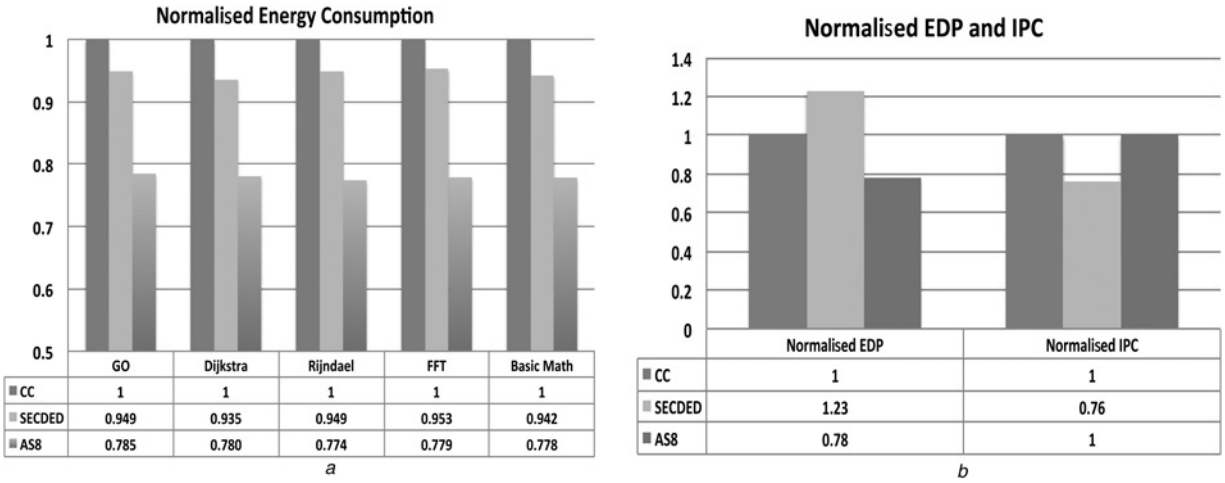


Fig. 9 *Energy and performance results for a set of embedded benchmarks*

a Energy consumption results of a 16 kB cache using: regular SRAM, AS8-SRAM, SECDED for a set of embedded benchmarks
b Average normalised EDP and IPC of the different architectures compared to a conventional cache

5.3 System level energy consumption

In this section, experiments are conducted to verify the effectiveness of the proposed architecture at a higher abstraction level. To quantify the system level energy consumption, we modified Simplescalar 3.0 [25] extensively to support the tested architectures. Thereafter, WATTCH [26], a Simplescalar-based power simulator was modified by estimating the cycle-accurate power consumption using HSPICE results in order to get accurate power estimations. The power oriented modifications track the accessed cells at run-time and compute the power values, cycle-by-cycle, based on the hardware configuration and the SPICE simulation results. In order to carry out a fair comparison, we constrain that the tested caches have an equal failure rate. Since the conventional 6T-SRAM cache (CC) is the least reliable, it is run at nominal supply voltage while the voltage reduction is applied to the other architectures, such that POF of all three caches are same at the respective V_{dd}. For this evaluation, we used benchmarks from two sets of embedded applications, namely the SPEC CPU2000 benchmark suite [27] and MiBench [28]. All benchmarks are compiled with Compaq alpha compiler using −O4 flag for Alpha 21264 ISA and the results correspond to a 16 kB 4-way associative data cache memory running at a frequency of 1 GHz.

Fig. 9*a* shows that for a considered POF, an AS8-SRAM-based cache memory consumes an average of 22% less energy than a conventional cache and 16% less than SECDED while insuring the same reliability level for iso-area. However, as SECDED needs additional circuitry, it negatively impacts the delay and decreases the whole processor performance. In fact, as shown in Fig. 9*b*, AS8-SRAM has higher EDP reduction than SECDED with no loss in terms of instructions per cycle (IPC).

6 Conclusion

In this paper, we proposed AS8-SRAM, a new 8-transistors asymmetric cell to protect SRAMs from soft errors. At circuit level, the proposed architecture increases memory cells critical charge and reinforces the storage element resistance to bit flips. At system level, our experiments on embedded benchmarks show that AS8-SRAM has the advantage of maintaining a reasonable reliability level at decreased supply voltage. We demonstrated that AS8-SRAM-based cache memory shows lower probability of failure compared to SECDED. Moreover, energy-oriented results demonstrate that the proposed architecture reduces total energy consumption by up to 22% over conventional caches without any considerable loss in terms of IPC. Future work will explore the possibility of combining AS8-SRAM with other techniques for higher reliability enhancement.

7 References

1 Ziegler, J.F., Curtis, H.W., Muhlfeld, H.P., *et al.*: 'IBM experiments in soft fails in computer electronics', *IBM J. Res. Dev.*, 1996, **40**, (1), pp. 3–18
2 Semiconductor industry association, international technology roadmap for semiconductors. Available: http://www.itrs.net
3 Anghel, L., Nicolaidis, M.: 'Cost reduction and evaluation of a temporary faults detecting technique'. Design, Automation and Test in Europe Conf. and Exhibition 2000, ser. DATE, 2000
4 Reviriego, P., Maestro, J.A., Flanagan, M.F.: 'Error detection in majority logic decoding of euclidean geometry low density parity check (eg-ldpc) codes', *IEEE Trans. VLSI Syst.*, 2013, **21**, (1), pp. 156–159
5 Guena, P.: 'A cache primer', Application Note, Freescale Semiconductors, 2004
6 Gherman, V., Evain, S., Seymour, N., *et al.*: 'Generalized parity-check matrices for sec-ded codes with fixed parity'. IEEE 17th Int. On-Line Testing Symp. (IOLTS), 2011, July 2011, pp. 198–201

7 Chakraborty, A., Homayoun, H., Khajeh, A., *et al.*: 'E mc2: Less energy through multi-copy cache'. Proc. 2010 Int. Conf. on Compilers, Architectures and Synthesis for Embedded Systems, ser. CASES '10, 2010
8 Alouani, I., Niar, S., Kurdahi, F., *et al.*: 'Parity-based mono-copy cache for low power consumption and high reliability'. 23rd IEEE Int. Symp. on Rapid System Prototyping (RSP), 2012, October 2012
9 Argyrides, C., Pradhan, D., Kocak, T.: 'Matrix codes for reliable and cost efficient memory chips', *IEEE Trans. Very Large Scale Integr. Syst.*, 2011, **19**, (3), pp. 420–428
10 Gherman, V.: 'Soft-error protection of tcams based on eccs and asymmetric sram cells', *Electron. Lett.*, 2014, **50**, pp. 1823–1824(1), Available: http://digital-library.theiet.org/content/journals/10.1049/el.2014.2540
11 Nisar, M.M., Barlas, I., Roemer, M.: 'Analysis and asymmetric sizing of cmos circuits for increased transient error tolerance'. AIAA Infotech@Aerospace 2010, Atlanta, Georgia, 2010
12 Torrens, G., Bota, S., Alorda, B., *et al.*: 'An experimental approach to accurate alpha-SER modeling and optimization through design parameters in 6T SRAM cells for deep-nanometer CMOS', *IEEE Trans. Device Mater. Reliab.*, 2014, **14**, (4), pp. 1013–1021
13 Gill, B.S., Papachristou, C., Wolff, F.G.: 'A new asymmetric sram cell to reduce soft errors and leakage power in fpga'. Design, Automation and Test in Europe Conf. and Exhibition 2007, ser. DATE'07, April 2007
14 Liu, X., Pan, L., Zhao, X., *et al.*: 'A novel soft error immunity sram cell'. IEEE Int. Integrated Reliability Workshop Final Report, 2013, ser. IRW '13, October 2013
15 Jahinuzzaman, S.M., Sharifkhani, M., Sachdev, M.: 'An analytical model for soft error critical charge of nanometric srams', *IEEE Trans. Very Large Scale Integr. Syst.*, 2009, **17**, (9), pp. 1187–1195
16 Lin, S., Kim, Y.-B., Lombardi, F.: 'A 11-transistor nanoscale cmos memory cell for hardening to soft errors', *IEEE Trans. Very Large Scale Integr. Syst.*, 2011, **19**, (5), pp. 900–904
17 Lin, S., Kim, Y.-B., Fabrizio, L.: 'Analysis and design of nanoscale cmos storage elements for single-event hardening with multiplenode upset', *IEEE Trans. Device Mater. Reliab.*, 2012, **12**, (1), pp. 68–77
18 Guo, J., Xiao, L., Mao, Z.: 'Novel low-power and highly reliable radiation hardened memory cell for 65 nm cmos technology', *IEEE Trans. Circuits Syst. I, Regul. Pap.*, 2014, **61**, (7), pp. 1994–2001
19 Ishikura, S., Kurumada, M., Terano, T., *et al.*: 'A 45 nm 2-port 8T-SRAM using hierarchical replica bitline technique with immunity from simultaneous r/w access issues', *IEEE J. Solid-State Circuits*, 2008, **43**, (4), pp. 938–945
20 Roche, P., Palau, J.M., Tavernier, C., *et al.*: 'Determination of key parameters for seu occurrence using 3-d full cell sram simulations', *IEEE Trans. Nucl. Sci.*, 1999, **46**, (6), pp. 1354–1362
21 Hazucha, P., Svensson, C.: 'Impact of cmos technology scaling on the atmospheric neutron soft error rate', *IEEE Trans. Nucl. Sci.*, 2000, **47**, (6), pp. 2586–2594
22 Predictive technology model (ptm) website. Available at: http://ptm.asu.edu
23 Jahinuzzaman, S.: 'Modeling and mitigation of soft errors in nanoscale srams'. PhD dissertation, University of Waterloo, 2008
24 Flautner, K., Kim, N.S., Martin, S., *et al.*: 'Drowsy chaches: simple techniques for reducing leakage power'. IEEE Int. Symp. on Computer Architecture, ser. ISCA '02, 2002
25 Austin, T., Larson, E., Ernst, D.: 'Simplescalar: an infrastructure for computer system modeling'. IEEE Computer, February 2002, vol. 35, no. 2
26 Brooks, V.T.D., Martonos, D.: 'Wattch: a framework for architecture level power analysis and optimizations'. Proc. Int. Symp. of Computer Architecture, 2000
27 Spec cpu2000 benchmarks. Available at: http://www.spec.org/cpu2000/index.html
28 Guthaus, M.R., Ringenberg, J.S., Ernst, D., *et al.*: 'Mibench: A free, commercially representative embedded benchmark suite'. Proc. Workload Characterization 2001. WWC-4. 2001 IEEE Int. Workshop, 2001